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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Anatoliy V. Tsyrganovich

Assignee: ZiLOG, Inc.

Title: "Frequency Locked Loop"

Serial No.: 10/690,874 Filed: October 21, 2003

Examiner: unknown Art Unit: 2817

Docket No.: ZIL-521-1P

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May 24, 2004

COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT PURSUANT  
TO 37 C.F.R. § 1.98**

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant brings six documents listed on the enclosed form PTO-1449 to the attention of the Examiner in the above-identified application. Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant application;
2. a representation that a search has been made; or
3. an admission that the information cited is, or is considered to be, material to patentability as defined in §1.56(b).

Applicant: Anatoliy V. Tsyrganovich  
Serial No.: 10/690,874  
Docket No.: ZIL-543-1P

Copies of the six documents listed on form PTO-1449 are enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on	
May 24, 2004,	
Darien K. Wallace	
	5/24/04
Signature	Date of Signature

Respectfully submitted,



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U.S. Department of Commerce, Patent and Trademark Office	Serial Number: 10/690,874
	Filing date: October 21, 2003
<b>TYPE</b> INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventor: Anatoliy V. Tsyrganovich
<b>MAY 27 2004</b> <i>PATENT &amp; TRADEMARK OFFICE</i>	Group Art Unit: 2817
Frequency Locked Loop	Examiner name: Unknown
	Attorney Docket No. ZIL-521-1P

**U.S. Patent Documents**

*Examiner Initial		Number	Date	Applicants	Class	Subclass	Filing Date, If Appropriate
	A	6,166,606	12/26/2000	Tsyrganovich	331	25	2/10/1999
	B	6,356,158	3/12/2002	Lesea	331	11	5/2/2000

### Foreign Patent Documents

**OTHER ART** (Including Author, Title, Date, Pertinent Pages, Etc.)

C	G. Fairhurst, "Phase Locked Loop (PLL)," United Kingdom, dated 1/10/2001, downloaded on 5/24/2004 from <a href="http://www.erg.abdn.ac.uk/users/gorry/course/phy-pages/dpll.html">http://www.erg.abdn.ac.uk/users/gorry/course/phy-pages/dpll.html</a> , 2 pages.
D	T. Olsson and Peter Nilsson, "An all-Digital PLL Clock Multiplier," Dept of Electroscience, Lund University, Lund, Sweden, date unknown (perhaps 2002), downloaded on 5/24/2004 from <a href="http://www.ap-asic.org/2002/proceedings/5B/5B-3.PDF">http://www.ap-asic.org/2002/proceedings/5B/5B-3.PDF</a> , 4 pages.
E	T. Olsson and Peter Nilsson, "A Digital PLL made from Standard Cells," Dept of Electroscience, Lund University, Lund, Sweden, date unknown (perhaps 2002), downloaded on 5/24/2004 from <a href="http://kontoret.webmaster.se/dockeeperfiles/340/887/A%20Digital%20PLL%20made%20from%20Standard%20Cells.pdf">http://kontoret.webmaster.se/dockeeperfiles/340/887/A%20Digital%20PLL%20made%20from%20Standard%20Cells.pdf</a> , 4 pages.
F	D. Abramovitch, "Lyapunov Redesign of Classical Digital Phase-Lock Loops," Agilent Labs, Palo Alto, CA, dated June 5, 2003, downloaded on 5/24/2004 from <a href="http://www.labs.agilent.com/personal/Danny.Abramovitch/pubs/lpll_cdig_talk.pdf">http://www.labs.agilent.com/personal/Danny.Abramovitch/pubs/lpll_cdig_talk.pdf</a> , 22 pages.

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.